IN THE CLAIMS

1. (Currently amended) A integrated circuit comprising:

a plurality of pairs of latches ~~(L1, L2)~~ being respectively clocked by two non-overlapping clock signals ~~(.PHI.1, .PHI.2)~~; and

delay circuits are placed between clock inputs of latches of a same clock signal, wherein each delay circuit drives more than one latch;

wherein a small proportion of a total number of latches to be switched during a cycle of a given clock signal are driven by the same delay circuit, thereby reducing substrate bounce.

2. (Canceled)

3. (Canceled)